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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/701,321 | 11/04/2003 | Joung-Yeal Kim | 5649-1169 | 5300 |

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| EXAMINER | |
|---|---|
| TRAN, ANH Q | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AIC

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/701,321 | KIM, JOUNG-YEAL | |
| | Examiner | Art Unit | |
| | Anh Q. Tran | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *50-55* is/are allowed.

6)☒ Claim(s) *1,10-13,21-26,30,31,33,34,38,39 and 41* is/are rejected.

7)☒ Claim(s) *2-9,14-20,27-29,32,35-37,40 and 42-49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 10-13, 21-26, 30-31, 33-34, 38-39, 41 are rejected under 35 U.S.C. 102(e) as being anticipated by Moyal (6,329,840).

Moyal shows:

1. A buffer circuit comprising:

an output terminal (124, Fig. 7);

a pull-up transistor (M17) connected between the output terminal and a supply voltage (connected to 132), wherein the pull-up transistor pulls the output terminal up to the supply voltage responsive to a pull-up control signal (CNT1);

a pull-down transistor (M18) connected between the output terminal and a reference voltage (connected to 134), wherein the pull-down transistor pulls the output terminal down to the reference voltage responsive to a pull-down control signal (CNT2);

a first logic gate (128a) configured to generate the pull-up control signal at a first output node responsive to a control signal (TRI-STATE+) and a data signal (A-), and

wherein the first logic gate includes a plurality of serially connected transistors (M1-M2) in an electrical path between the supply voltage and the first output node; and

a second logic gate (128b) configured to generate the pull-down control signal at a second output node responsive to the data signal and an inverse of the control signal (TRI-STATE-) and wherein the second logic gate includes a plurality of serially connected transistors (M9-M10) in a path between the supply voltage and the second output node;

wherein the number of serially connected transistors in the path between the supply voltage and the first output node is equivalent to the number of serially connected transistors in the path between the supply voltage and the second output node.

10. A buffer circuit according to Claim 1 wherein the reference voltage comprises a ground voltage (ground, col. 5, line 2).

11. A buffer circuit according to Claim 1 wherein the first logic gate comprises a NAND gate (M1-M6) and wherein the second logic gate comprises a NOR gate (M9-M14).

12. A buffer circuit according to Claim 1 wherein the plurality of serially connected transistors in the path between the supply voltage and the first output node are PMOS transistors, and wherein the plurality of serially connected transistors in the path between the supply voltage and the second output node are PMOS transistors (col. 4, lines 26-67).

13. An output buffer comprising:

an output terminal (124, Fig. 7);

a pull-up transistor (M17) connected between the output terminal and a supply voltage, wherein the pull-up transistor pulls the output terminal up to the supply voltage responsive to a pull-up control signal (CNT1);

a pull-down transistor (M18) connected between the output terminal and a reference voltage, wherein the pull-down transistor pulls the output terminal down to the reference voltage responsive to a pull-down control signal;

a first logic gate (128a) configured to generate the pull-up control signal at a first output node responsive to a control signal (TRI-STATE+) and a data signal (A-), and wherein the first logic gate includes a plurality of serially connected transistors (M3-M4) in a path between the first output node and the reference voltage; and

a second logic gate (128b) configured to generate the pull-down control signal at a second output node responsive to the data signal and an inverse (TRI-STATE-) of the control signal and wherein the second logic gate includes a plurality of serially connected transistors (M11-M12) in a path between the second output node and the reference voltage;

wherein the number of serially connected transistors in the path between the first output node and the reference voltage is equivalent to the number of Serially connected transistors in the path between the second output node and the reference voltage.

22. A buffer circuit according to Claim 13 wherein the reference voltage comprises a ground voltage (ground, col. 5, line 2).

23. A buffer circuit according to Claim 13 wherein the first logic gate comprises a NAND gate (M1-M6) and wherein the second logic gate comprises a NOR gate (M9-M14).

24. A buffer circuit according to Claim 13 wherein the plurality of serially connected transistors in the path between the supply voltage and the first output node are NMOS transistors, and wherein the plurality of serially connected transistors in the path between the supply voltage and the second output node are NMOS transistors (col. 4, lines 26-67).

25. A buffer circuit comprising:

an output terminal (124);

a pull-up transistor (M17) connected between the output terminal and a supply voltage (VCC), wherein the pull-up transistor pulls the output terminal up to the supply voltage responsive to a pull-up control signal (CNT1);

a pull-down transistor (M18) connected between the output terminal and a reference voltage (VSS), wherein the pull-down transistor pulls the output terminal down to the reference voltage responsive to a pull-down control signal (CNT2);

a first logic gate (128a) configured to generate the pull-up control signal at a first output node responsive to a control signal (TRI-STATE+) and a data signal (A-), and wherein the first logic gate includes first (M2) and second transistors (M5) connected in parallel between the supply voltage and the first output node and third (M3) and fourth transistors (M8) connected in parallel between the first output node and the reference voltage; and

a second logic gate (128b) configured to generate the pull-down control signal at a second output node responsive to the data signal and an inverse of the control signal.

26. A buffer circuit according to Claim 25 wherein the first and second transistors comprises PMOS transistors and wherein the third and fourth transistors comprise NMOS transistors (col. 4).

30. A buffer circuit according to Claim 25 wherein the second logic gate includes fifth (M10) and sixth transistors (M13) connected in parallel between the supply voltage and the second output node and seventh (M11) and eighth transistors (M14) connected in parallel between the second output node and the reference voltage.

31. A buffer circuit according to Claim 30 wherein first and second and fifth and sixth transistors comprise PMOS transistors, and wherein the third and fourth and seventh and eighth transistors comprise NMOS transistors (col. 4).

The limitations of claims 33-34, 38-39, 41 are rejected as above.

***Allowable Subject Matter***

3. Claims 2-9, 14-20, 27-29, 32, 35-37, 40, 42-49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 50-55 are allowed.

5. The following is an examiner's statement of reasons for allowance:

elements are connected as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

3/3/05